

FIG. 1 prior art

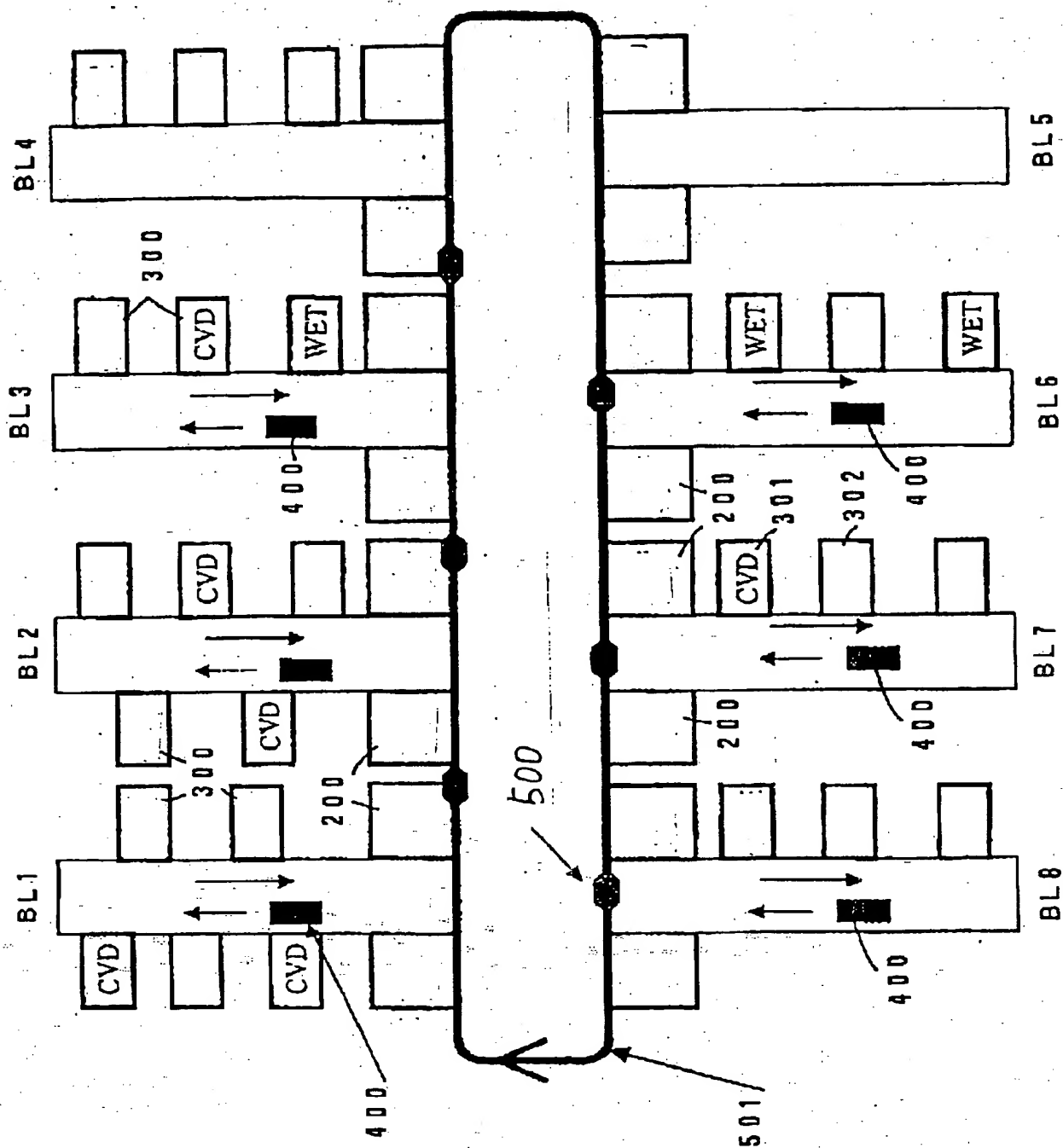
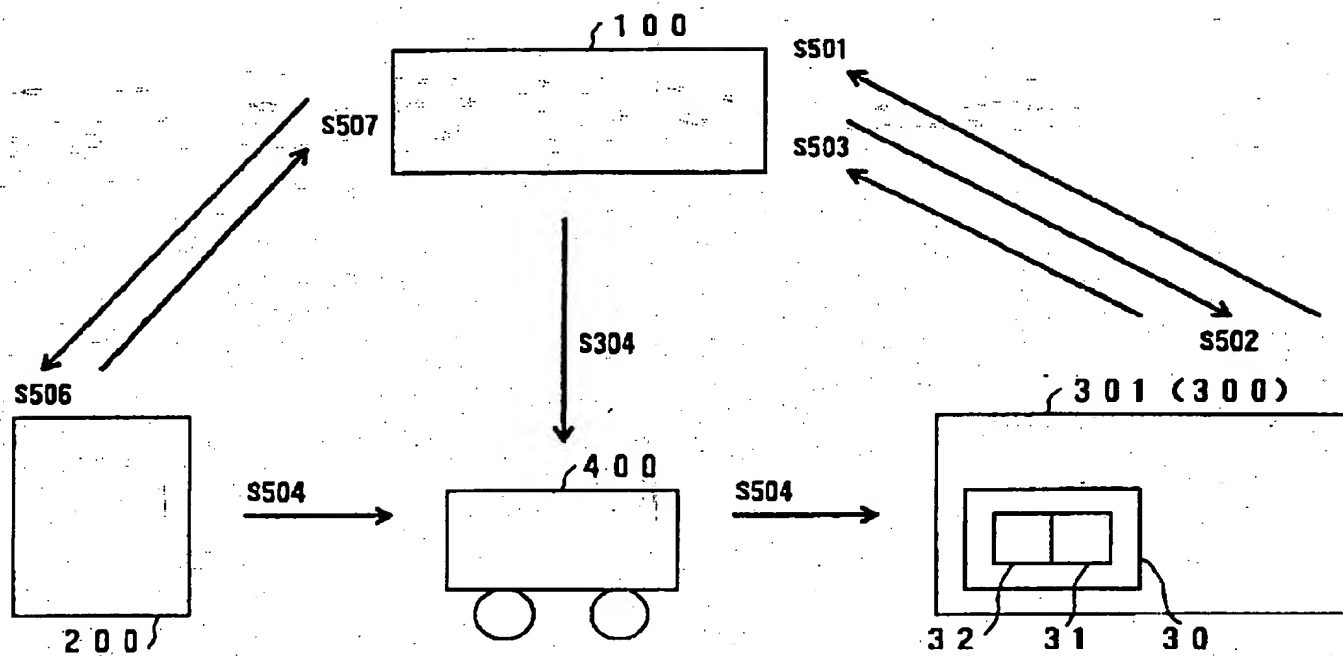


FIG. 2 prior art



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FIG. 3

low pressure CVD system

host computer

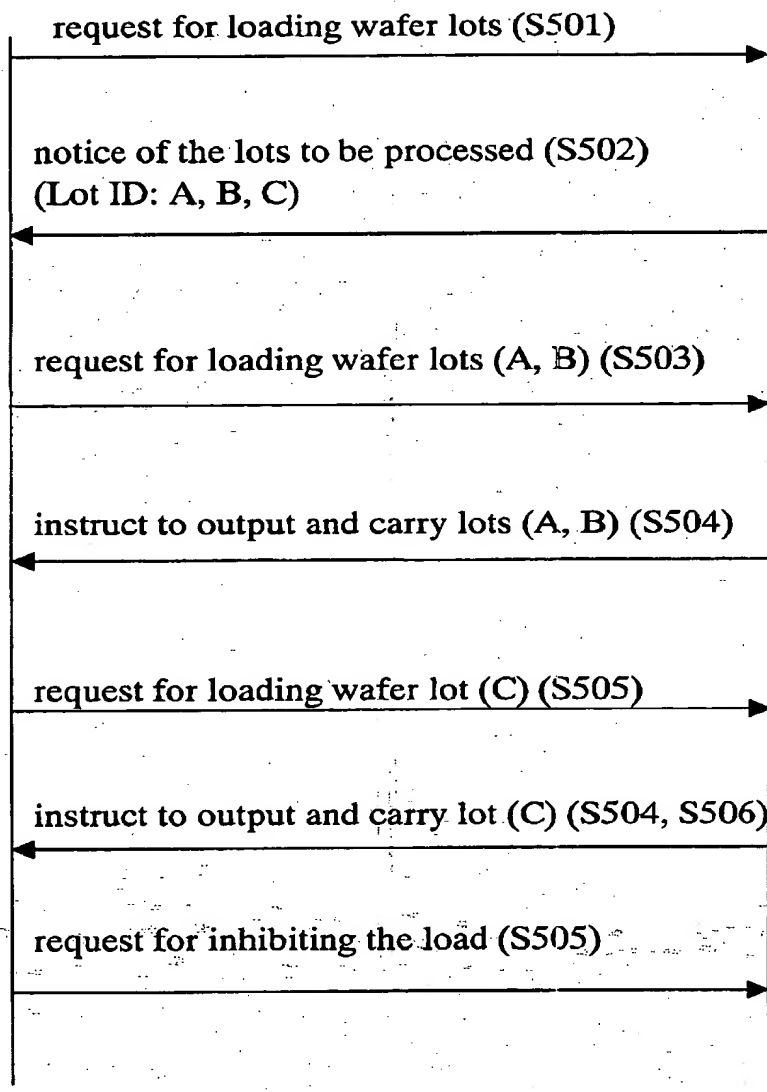
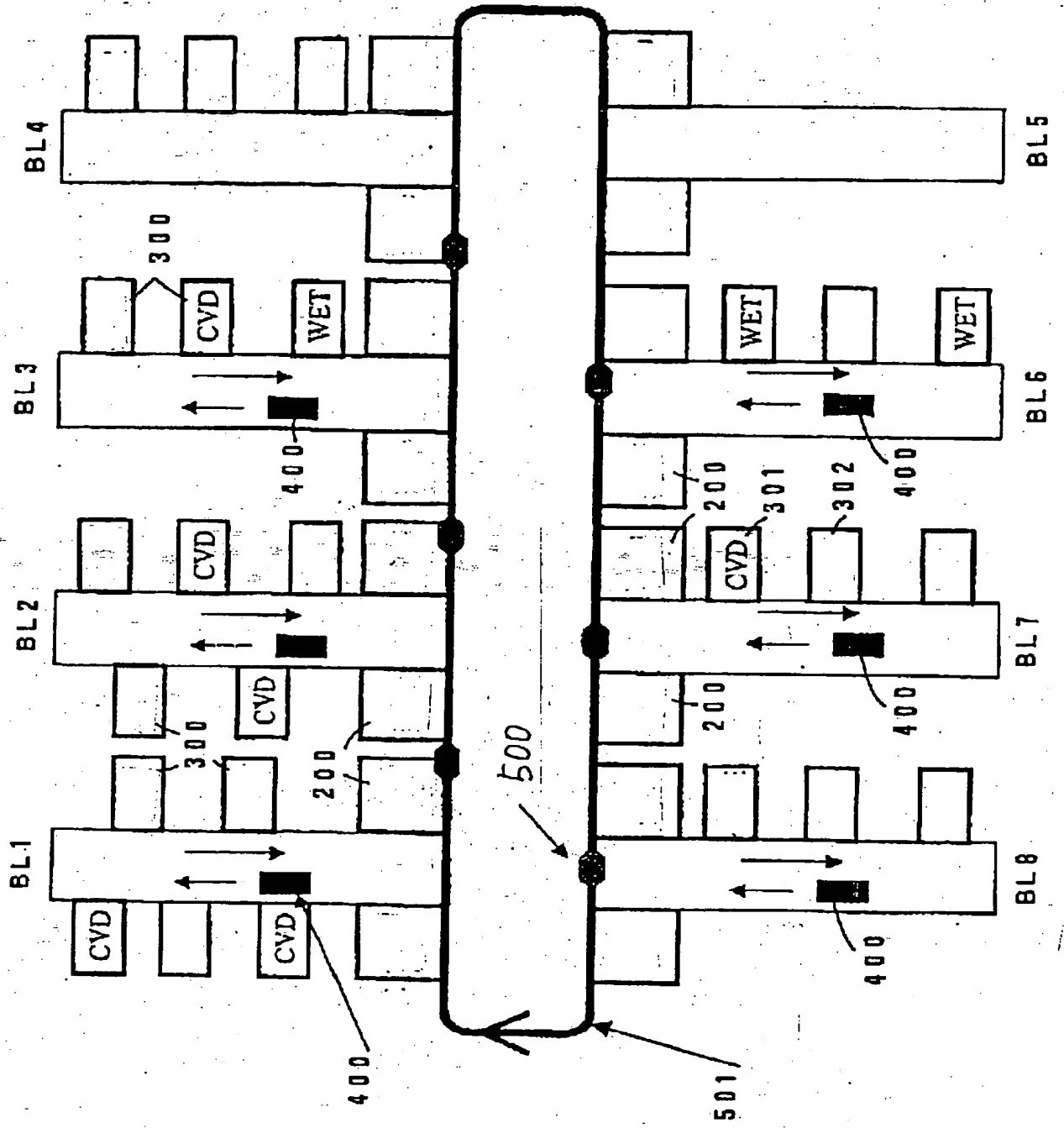
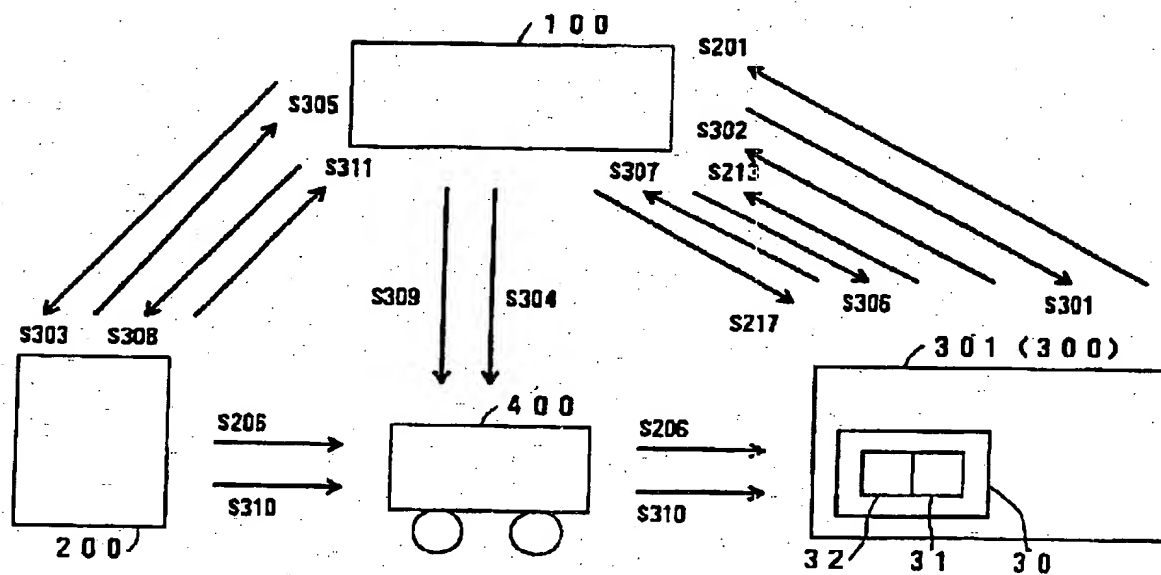
timer set  
time period

FIG. 4



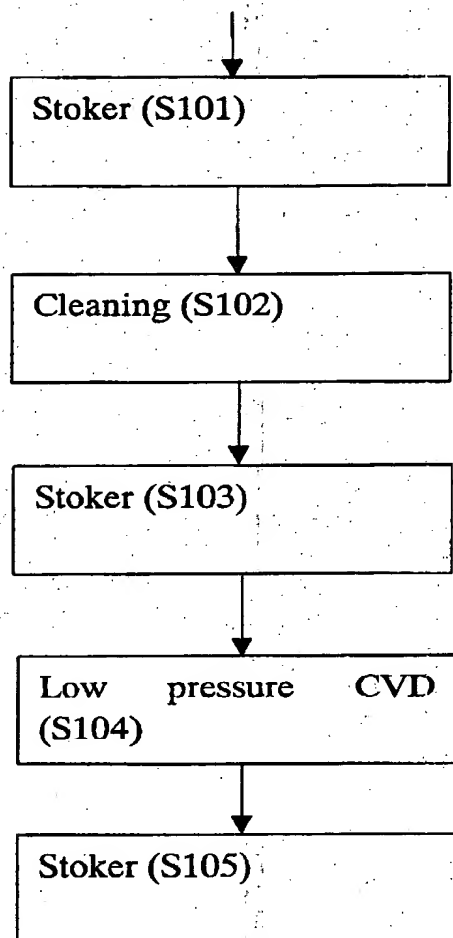
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FIG. 5



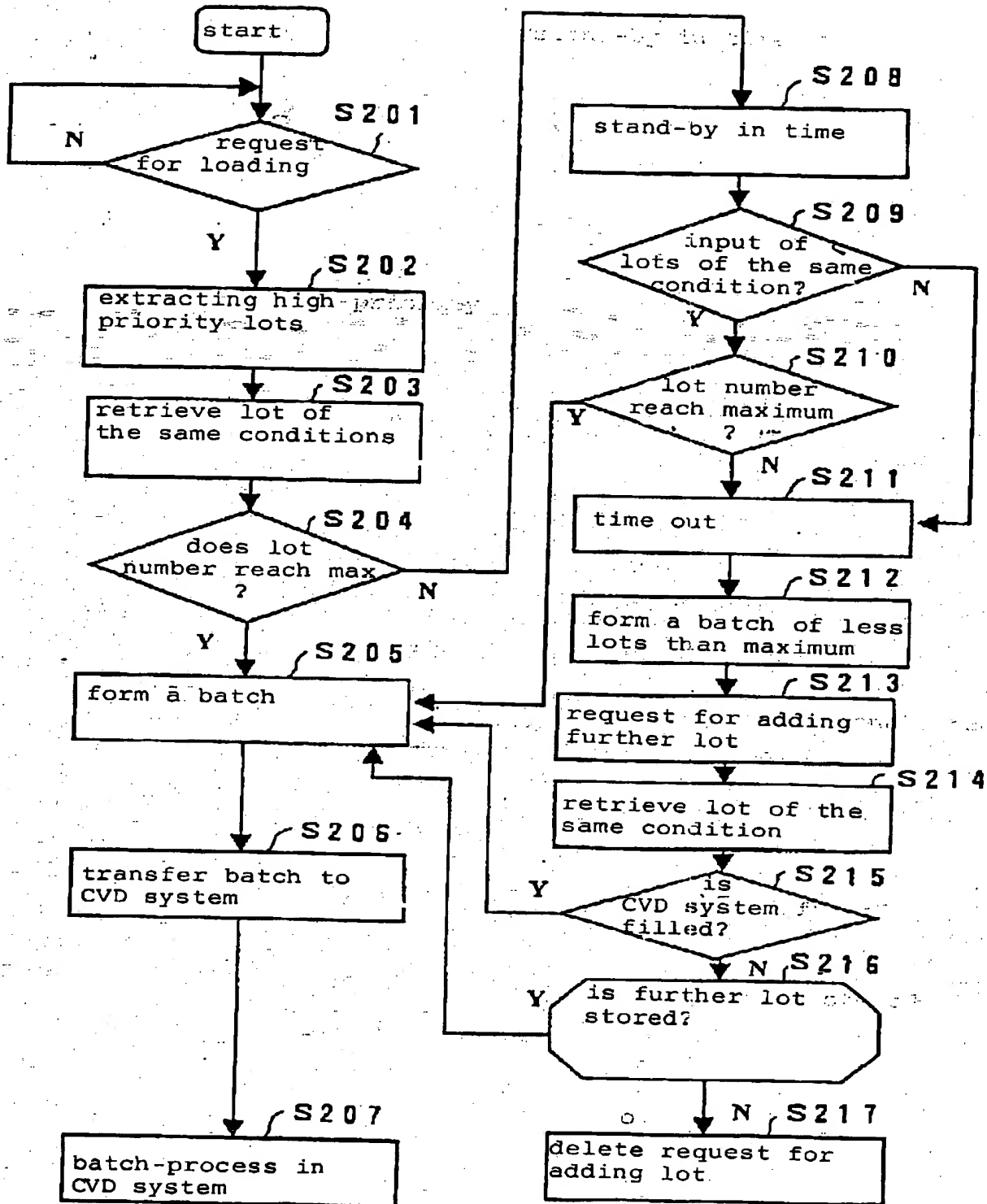
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FIG. 6



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FIG. 7

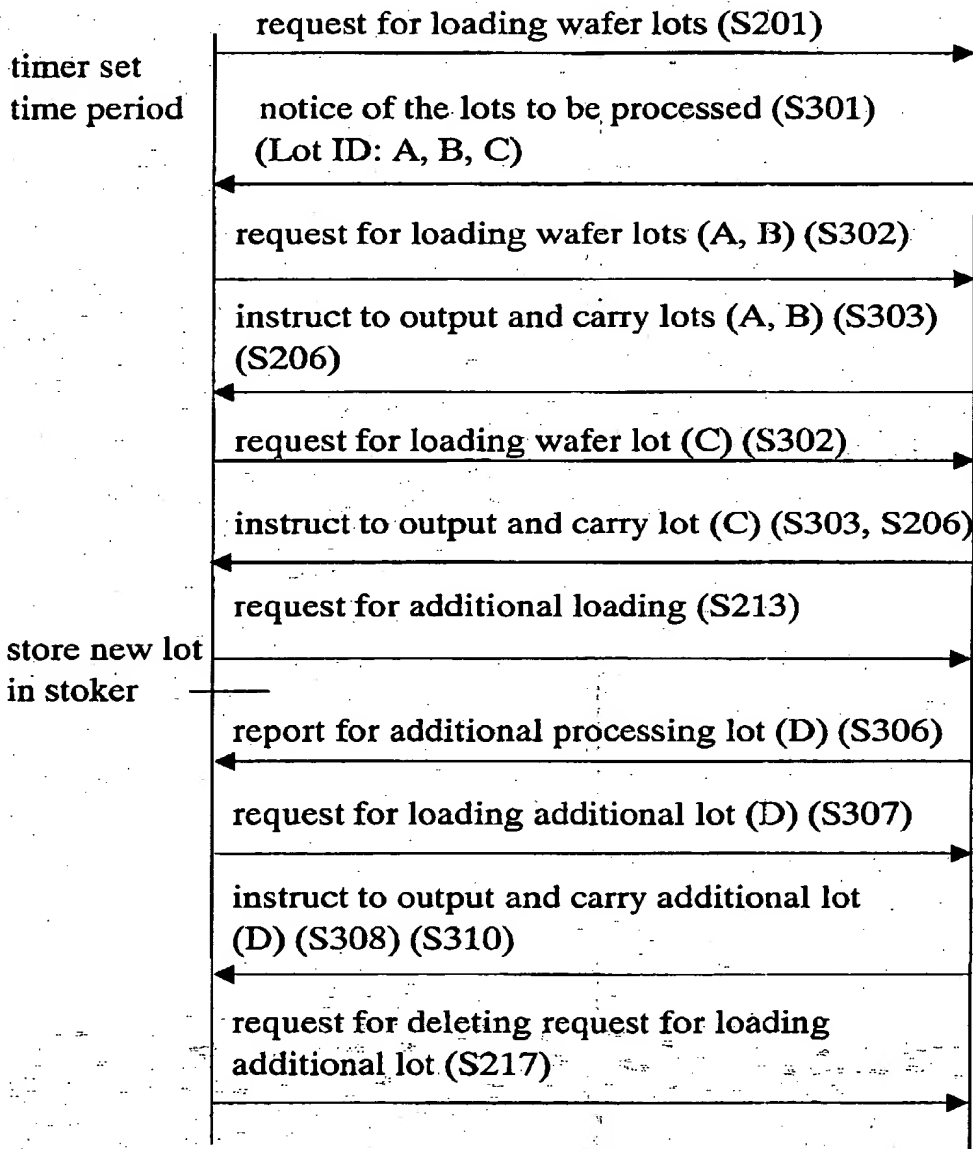


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FIG. 8

low pressure CVD system

host computer



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FIG. 9

